Davis Cheung

SILICON ENGINEER

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Hard-working engineer seeks new opportunities

I'm a full-time engineer looking for exciting new positions in the field of computer hardware and software. With strong foundations in full-stack development, pre-silicon design verification, and low-level programming; I'm looking for a role where I can leverage my skills to build beautiful, well-organized systems.

FEATURED PROJECTS

Personal VPN w/ Active-probing Defence / Debian Linux, VLESS, ACME

Setup and deployed a VLESS TCP XTLS-Vision REALITY VPS for personal use. The server features fallback mechanisms to defend against active-probing, as well as REALITY and uTLS for disguising traffic as unblocked external sites.

Runtime RTL Assertion System / SystemVerilog, UVM, C/C++, VPI, Ruby

Created an assertion system leveraging **SystemVerilog**, **UVM**, and **VPI (PLI 2.0)** to dynamically generate UVM event-based assertions at runtime, bypassing **7+ hour** build & simulation compilation times while greatly reducing code bloat.

Real-time Fluid Simulator / Unity, C#, HLSL (High-Level Shader Language)

Created a real-time Lagrangian fluid sim with physics kernels in **HLSL**. Optimized for **locality, occupancy,** and **algorithmic efficiency** to achieve real-time performance on large-scale sims (up to **1 mil.** particles). **Won best poster.**

EXPERIENCE

2023 - 2024; 2025-Presenmt

SOC Design Verification / AMD (MI Instinct GPU's)

- Organized test planning for SOC RAS (ECC) features across the chip
- Wrote **UVM** components, **testbench** checkers, and testcases for verifying chiplet reset, ECC, and error recovery features
- Debugged **AXI** and internal data port communication flows across dies and for a wide range of functional traffic using **Synopsys Verdi**
- Engaged with deployment teams, IP teams, and architects to resolve connectivity issues and fix RTL bugs
- Developed various text-parsing scripts (**Python, Perl, Ruby**) for verifying connectivity, parsing errors, and generating verif components
- Deployed **high ROI**, lightweight **UVM monitors** for ensuring that global parity in all chiplets were functioning as expected
- Brought-up and debugged various **traffic stimulus/sequencers** for use in **error recovery** scenarios, including various forms of chip-wide **reset**

2022

Software Prototyper / Science Discovery Zone (SDZ)

- Wrote front-end and back-end elements of Bootstrap/Django(**Python**)/MySQL and React/Express.js(Node.js)/PostgreSQL stacks
- Overhauled back-end web models to leverage object-oriented model-template-views (MTVs)
- Wrote a **Python**-based **web crawler** and **scraper** for automatically querying and scanning pages for keywords, parsing relevant data as needed across several sites

EDUCATION

B.Eng. Computer Engineering
Ryerson University, 2020-2025
GPA: **4.1** / 4.3

TECHNICAL SKILLS

Programming Languages

- Ruby, Perl, Python, **C/C++**, Java, SystemC, Verilog, **SystemVerilog,** VHDL

Frameworks & Libraries

- **UVM, VCS (RTL simulation)**
- Node.js/Express.js, Django, Flask, PHP, React, Redis, SQL, HTML/CSS

Other

- OpenCV, MATLAB, **Linux/UNIX**
- SolidWorks, Quartus, **Verdi, nWave**

AWARDS

- **AMD Quarterly Spotlight Award 2026**
- **Dean's List**, 2019-2025
- Queens' Gordon and Agnes Brash Award (Scholarship)

COOL STUFF I'VE MADE